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High-Efficiency Bidirectional Buck-Boost Converter for Photovoltaic and Energy Storage Systems in a Smart Grid

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***Abstract*—This paper proposes a new bidirectional buck-boost converter, which is a key component in a photovoltaic and energy storage system (PV-ESS). Conventional bidirectional buck-boost converters for ESSs operate in discontinuous conduction mode (DCM) to achieve zero-voltage-switching turn-on for switches. However, operation in DCM causes high ripples in the output voltage and current, as well as low power-conversion efficiency. To improve on the performance of the conventional converter, the proposed converter has a new combined structure of a cascaded buck-boost converter and an auxiliary capacitor. The combined structure of the proposed converter reduces the output current ripple by providing a current path and the efficiency is increased. A prototype was built and tested to verify the effectiveness of the converter. The proposed converter has a maximum efficiency of 98%, less than 5.14 $V_{p.p}$ of output voltage ripple, and less than 7.12 $A_{p.p}$ of output current ripple. These results were obtained at an input voltage of 160 V, switching frequency of 45 kHz, output voltage of 80 ~ 320 V, and output power of 16 ~ 160 W. The experimental results show that the proposed converter has improved performance compared to the conventional converter.**

***Index Terms*—DC-DC power conversion, Energy storage, Pulse width modulated power converters.**

I. Introduction

SMART grid (Fig. 1) is future electric energy system that has been studied to reduce mismatching between sources of electricity (such as renewable energy and power plants) and electricity consumers (homes, vehicles, factories, etc.). However, the energy production of renewable energy depends on environmental conditions. Therefore, an energy storage system (ESS) is needed in a smart grid to provide stability and efficiently manage the renewable energy [1-3].

An ESS consists of a battery that stores electric energy and a bidirectional DC-DC converter that transfers energy from the battery and renewable energy source in both directions [4-9]. A conventional bidirectional DC-DC converter uses a half-bridge converter with two switches based on a buck or boost DC-DC converter. In the buck mode of the converter, electric energy is transferred from a high voltage (HV) port to the low voltage (LV) port. In boost mode, the electric energy is transferred from the LV port to the HV port. The conventional bidirectional converter has a limitation in that it can only be operated in buck mode in one direction and boost mode in the other direction (Fig. 2(a) and Fig. 2(b)) [10-12]. Therefore, when the input is a photovoltaic (PV) module and the output is battery cells in a smart grid, a half bridge converter based on a buck or boost converter cannot be used because of the following reasons:

1) The battery cells repeatedly perform charging and discharging operations, resulting in large voltage variation [13, 14].

2) The PV module has a large voltage variation that depends on the module temperature and the solar irradiance [15-17]. Thus, the ranges of the input voltage and output voltage can

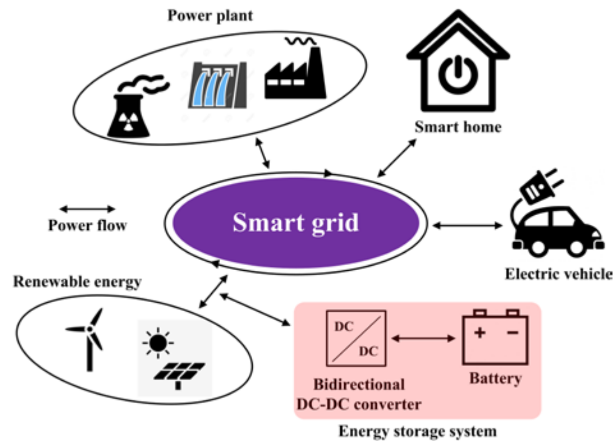

Fig. 1. Diagram of smart grid.

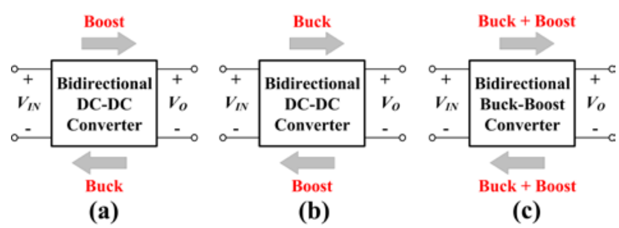

Fig. 2. Block diagrams in case of (a) $V_{IN} < V_O$, (b) $V_{IN} > V_O$, and (c) $V_{IN} < V_O$ & $V_{IN} > V_O$.

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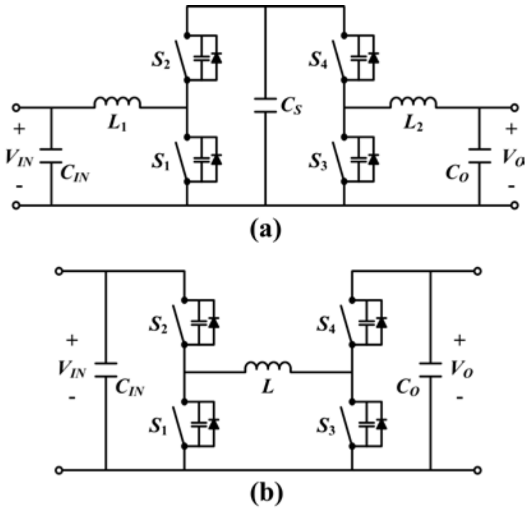

Fig. 3. Circuit structures of (a) Combined Half-Bridge (CHB) converter and (b) Cascaded Buck-Boost (CBB) converter.

overlap [18, 19].

Bidirectional buck-boost converters (Fig. 2(c)) were introduced for use in cases of overlapping input and output voltages [19-28]. They can operate in both buck and boost modes in both directions. A combined half-bridge (CHB) converter (Fig. 3(a)) is the most basic bidirectional buck-boost converter and has a symmetric structure with respect to the storage capacitor C_S [20, 21]. There is one inductor at the input port and one at the output port, which results in low voltage ripples in the input and output. However, because the CHB converter uses two inductors of the same size, it is large and has a low power-conversion efficiency η_e due to the DC-offset current of each inductor.

Cascaded buck-boost (CBB) converter (Fig. 3(b)), along with the CHB converter, has been commonly used in ESSs. Compared with the CHB converter, CBB converter is smaller and has higher η_e because it uses only one inductor L [19, 22-28]. Recently, research has been actively conducted on bidirectional buck-boost DC-DC converters in discontinuous conduction mode (DCM) because this mode can achieve zero-voltage-switching (ZVS) turn-on of the switches [19, 26-28]. However, operation in DCM increases the current ripple of L, which affects the output current ripple and increases the output voltage ripple.

In this paper, an enhanced CBB converter is proposed to improve on the performance of the conventional CBB converter. The proposed converter is targeted to a PV-ESS system that uses a micro-inverter, which has been widely used in a smart grid [29, 30]. The converter has a new combined structure of a CBB converter and an auxiliary capacitor. This structure can reduce the output voltage ripple and increase η_e by effectively reducing the output current ripple. The circuit structure and operating principle of the proposed converter are described in Section II, and design considerations are given in Section III. Experimental results are given in Section IV, and a conclusion is given in Section V.

II. Proposed DC-DC Converter

A. Circuit Structure

The proposed converter (Fig. 4) consists of a conventional CBB converter and an auxiliary capacitor (C_a), and has a symmetric structure with respect to C_a and L. The CBB converter consists of two capacitors (C_{IN}, C_O), four switches (S_1, S_2, S_3, S_4), and an inductor (L). Four switches (S_1, S_2, S_3, S_4) and an inductor (L) control the direction of energy transfer and the ratio between the input voltage and output voltage. Four switches are turned on in the ZVS condition by operating in DCM. Two capacitors (C_{IN}, C_O) reduce the output voltage ripple and noise, and an auxiliary capacitor (C_a) reduces the output current ripple by providing a current path.

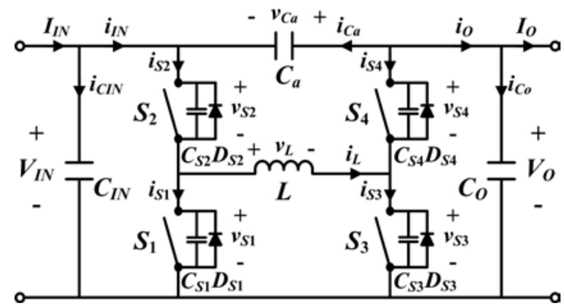

Fig. 4. Circuit structure of the proposed converter.

TABLE I
States of Switches in Six Operating Conditions

Six operating conditions		Switches			
Directions of energy transfer	**Types of the operation**	S_1	S_2	S_3	S_4
$V_{IN} \rightarrow V_O$	Buck	1 - D	D	0	1
	Buck-Boost	1 - D	D	D	1 - D
	Boost	0	1	D	1 - D
$V_O \rightarrow V_{IN}$	Buck	0	1	D	1 - D
	Buck-Boost	1 - D	D	D	1 - D
	Boost	1 - D	D	0	1

B. Principle of Operation

The proposed converter operates with a fixed switching period T_S and controls the voltage gain by changing the duty ratio D of the switches (S_1, S_2, S_3, S_4) from 0 to 1. Each switch has four states in six operating conditions created by the energy transfer directions between V_{IN} and V_O and the types of operation (buck, boost, and buck-boost), as shown in Table I. Due to the symmetric structure with respect to C_a and L, the operations are separated by only the types of operation in one direction of energy transfer ($V_{IN} \rightarrow V_O$).

To simplify the analysis of the operation, the following assumptions are made: 1) the inductor and all capacitors are lossless, 2) the voltage ripples of C_{IN}, C_a, and C_O are small enough to assume that V_{IN}, V_{Ca}, and V_O are constant voltage sources, and 3) the converter operates in steady state.

(1) *Buck mode*

When the proposed converter operates in buck mode, it has four distinct operating modes (*Mode* 1 ~ 4). The equivalent circuits and operating waveforms are shown in Fig. 5 and Fig. 6.

Mode 1 (Fig. 5(a), $t_0 \le t \le t_1$) starts when S_2 is turned on. At $t = t_0$, S_2 achieves ZVS turn-on because the body diode D_{S2} of S_2 is turned on before $t = t_0$. Then, the voltage v_L of L becomes $V_{IN} - V_O$, and the current i_L of L is expressed as

$$i_L(t) = i_L(t_0) + \frac{V_{IN} - V_O}{L}(t - t_0). \quad (1)$$

The current i_{S2} of S_2 is equal to i_L, so i_{S2} is expressed as

$$i_{S2}(t) = i_L(t_0) + \frac{V_{IN} - V_O}{L}(t - t_0).$$

In this mode, the current i_{Ca} of C_a, the current i_{Co} of C_O, the output current i_O, and the load current I_O have the following relations: $i_O = i_{Co} + I_O$, $i_{Co} = i_{Ca} \cdot C_O/C_a$, and $i_O = i_L - i_{Ca}$. Therefore, i_{Ca} and i_O can be derived as

$$i_{Ca}(t) = \frac{C_a}{C_a + C_O}\left[i_L(t) - I_O\right]$$

$$i_O(t) = \frac{C_O}{C_a + C_O} i_L(t) + \frac{C_a}{C_a + C_O} I_O. \quad (2)$$

The voltage v_{Ca} across the auxiliary capacitor C_a is expressed as

$$v_{Ca}(t) = V_{Ca} + \Delta v_{Ca,AC}(t)$$

where V_{Ca} and $\Delta v_{Ca,AC}$ represent the DC voltage and the AC ripple voltage across the C_a, respectively. Because $V_{Ca} >> \Delta v_{Ca,AC}$, v_{Ca} can be approximated as

$$v_{Ca}(t) \approx V_{Ca} = V_O - V_{IN}.$$

Mode 2 (Fig. 5(b), $t_1 \le t \le t_2$) starts when S_2 is turned off. At this time, S_1 remains in the off state to prevent a shoot-through problem with S_1 and S_2. In this mode, the output capacitor C_{S1} of S_1 discharges from V_{IN} to 0, and the output capacitor C_{S2} of S_2 charges from 0 to V_{IN}. Shortly after the discharging of C_{S1} and charging of C_{S2} are finished, the body diode D_{S1} of S_1 is turned on.

Mode 3 (Fig. 5(c), $t_2 \le t \le t_3$) starts with the ZVS turn-on of S_1 because D_{S1} is turned on before $t = t_2$. Then, v_L becomes $-V_O$, and thereby i_L is expressed as

$$i_L(t) = i_L(t_2) - \frac{V_O}{L}(t - t_2). \quad (3)$$

The current i_{S1} of S_1 is equal to $-i_L$, so i_{S1} is obtained as

$$i_{S1}(t) = -i_L(t_2) + \frac{V_O}{L}(t - t_2).$$

Because $i_O = i_L - i_{Ca}$, $i_O = i_{Co} + I_O$, and $i_{Co} = i_{Ca} \cdot C_O/C_a$, i_{Ca} and i_O are expressed as

$$i_{Ca}(t) = \frac{C_a}{C_a + C_O}\left[i_L(t) - I_O\right] \quad (4)$$

$$i_O(t) = \frac{C_O}{C_a + C_O} i_L(t) + \frac{C_a}{C_a + C_O} I_O. \quad (5)$$

Mode 4 (Fig. 5(d), $t_3 \le t \le t_4$) starts when S_1 is turned off and S_2 remains in the off state. In this mode, C_{S1} charges from 0 to V_{IN}, and C_{S2} discharges from V_{IN} to 0. Shortly after the charging of C_{S1} and discharging of C_{S2} are finished, D_{S2} is turned on.

At $t = t_0$, i_L has an initial value of $i_L(t_0)$, and $i_L(t_0)$ is obtained as follows: By inserting $t = t_2$ into (1), the current ripple Δi_L of i_L is obtained as

$$\Delta i_L = i_L(t_2) - i_L(t_0) = \frac{V_{IN} - V_O}{L} DT_S, \quad (6)$$

where $DT_S = t_2 - t_0$. The average current of L for one T_S is obtained as $<i_L> = I_O$ by applying the ampere-second balance law for capacitors to $i_L(t) = i_{Ca}(t) + i_{Co}(t) + I_O$. Then, $i_L(t_0) = <i_L> - \Delta i_L/2$ is represented as

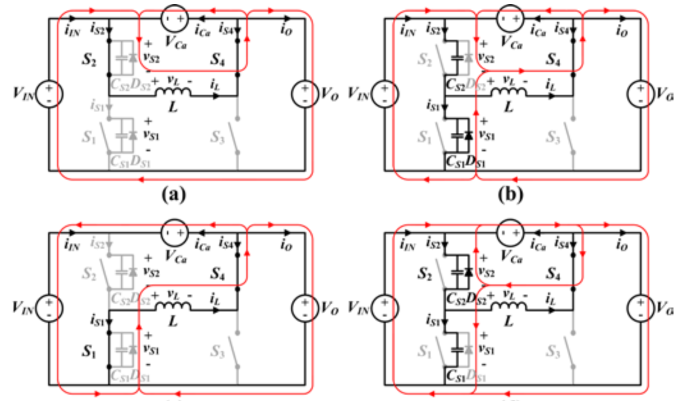

Fig. 5. Circuit diagrams for the operation of buck; (a) *Mode* 1, (b) *Mode* 2, (c) *Mode* 3, and (d) *Mode* 4.

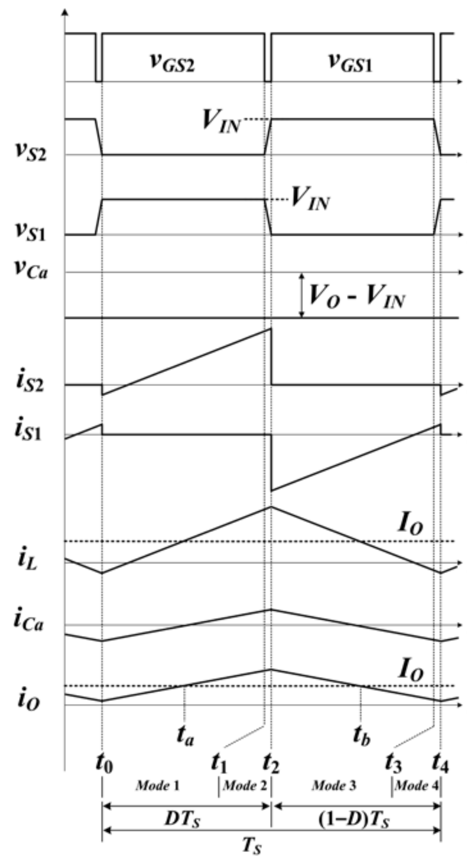

Fig. 6. Operational waveforms in the operation of buck.

$$i_L(t_0) = I_O - \frac{V_{IN} - V_O}{2L} DT_S, \quad (7)$$

and $i_L(t_2) = <i_L> + \Delta i_L/2$ is expressed as

$$i_L(t_2) = I_O + \frac{V_{IN} - V_O}{2L} DT_S. \quad (8)$$

(2) *Boost mode*

The boost operation also has four distinct operating modes (*Mode* 1 ~ 4), and the equivalent circuits and operating waveforms are shown in Fig. 7 and Fig. 8, respectively.

Mode 1 (Fig. 7(a), $t_0 \le t \le t_1$) starts when S_3 is turned on. At $t = t_0$, S_3 achieves ZVS turn-on because the body diode D_{S3} of S_3 is turned on before $t = t_0$. Then, v_L becomes V_{IN}, and i_L is expressed as

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$$i_L(t) = i_L(t_0) + \frac{V_{IN}}{L}(t - t_0). \quad (9)$$

The current i_{S3} of S_3 is the same as i_L, so i_{S3} is expressed as

$$i_{S3}(t) = i_L(t_0) + \frac{V_{IN}}{L}(t - t_0).$$

Because $i_O = -i_{Ca}$, $i_O = i_{Co} + I_O$, and $i_{Co} = i_{Ca} \cdot C_O/C_a$, i_{Ca} and i_O are expressed as

$$i_{Ca}(t) = -\frac{C_a}{C_a + C_O} I_O$$

$$i_O(t) = \frac{C_a}{C_a + C_O} I_O. \quad (10)$$

The voltage v_{Ca} across the auxiliary capacitor C_a is expressed as

$$v_{Ca}(t) = V_{Ca} + \Delta v_{Ca,AC}(t).$$

Because $V_{Ca} >> \Delta v_{Ca,AC}$, this expression can be approximated as

$$v_{Ca}(t) \approx V_{Ca} = V_O - V_{IN}$$

Mode 2 (Fig. 7(b), $t_1 \le t \le t_2$) starts when S_3 is turned off and S_4 remains in the off state. In this mode, the output capacitor C_{S3} of S_3 charges from 0 to V_O, and the output capacitor C_{S4} of S_4 discharges from V_O to 0. Shortly after the charging of C_{S3} and discharging of C_{S4} are finished, the body diode D_{S4} of S_4 is turned on.

Mode 3 (Fig. 7(c), $t_2 \le t \le t_3$) starts with the ZVS turn-on of S_4 because D_{S4} is turned on before $t = t_2$. Then, v_L becomes V_{IN} - V_O, and i_L is expressed as

$$i_L(t) = i_L(t_2) + \frac{V_{IN} - V_O}{L}(t - t_2). \quad (11)$$

The current i_{S4} of S_4 is equal to $-i_L$, so i_{S4} is obtained as

$$i_{S4}(t) = -i_L(t_2) - \frac{V_{IN} - V_O}{L}(t - t_2).$$

Because $i_O = i_L - i_{Ca}$, $i_O = i_{Co} + I_O$, and $i_{Co} = i_{Ca} \cdot C_O/C_a$, i_{Ca} and i_O are expressed as

$$i_{Ca}(t) = \frac{C_a}{C_a + C_O}\left[i_L(t) - I_O\right] \quad (12)$$

$$i_O(t) = \frac{C_O}{C_a + C_O} i_L(t) + \frac{C_a}{C_a + C_O} I_O. \quad (13)$$

Mode 4 (Fig. 7(d), $t_3 \le t \le t_4$) starts when S_4 is turned off and S_3 remains in off-state. In this mode, C_{S3} discharges from V_O to 0 and C_{S4} charges from 0 to V_O. Shortly after the discharging of C_{S3} and charging of C_{S4} are finished, D_{S3} is turned on.

By inserting $t = t_2$ into (9), Δi_L for boost operation is obtained as

$$\Delta i_L = i_L(t_2) - i_L(t_0) = \frac{V_{IN}}{L} DT_S, \quad (14)$$

where $DT_S = t_2 - t_0$. Because $\langle i_L \rangle = I_{IN}$ and $i_L(t_0) = \langle i_L \rangle - \Delta i_L/2$, $i_L(t_0)$ is expressed as

$$i_L(t_0) = I_{IN} - \frac{V_{IN}}{2L} DT_S. \quad (15)$$

$i_L(t_2) = \langle i_L \rangle + \Delta i_L/2$ is expressed as

$$i_L(t_2) = I_{IN} + \frac{V_{IN}}{2L} DT_S. \quad (16)$$

(3) *Buck-boost mode*

The buck-boost operation has four distinct operating modes (*Mode* 1 ~ 4), and the equivalent circuits and operating

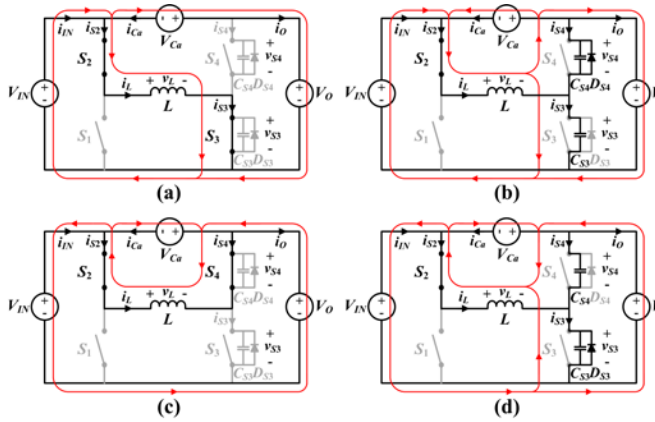

Fig. 7. Circuit diagrams for the operation of boost; (a) *Mode* 1, (b) *Mode* 2, (c) *Mode* 3, and (d) *Mode* 4.

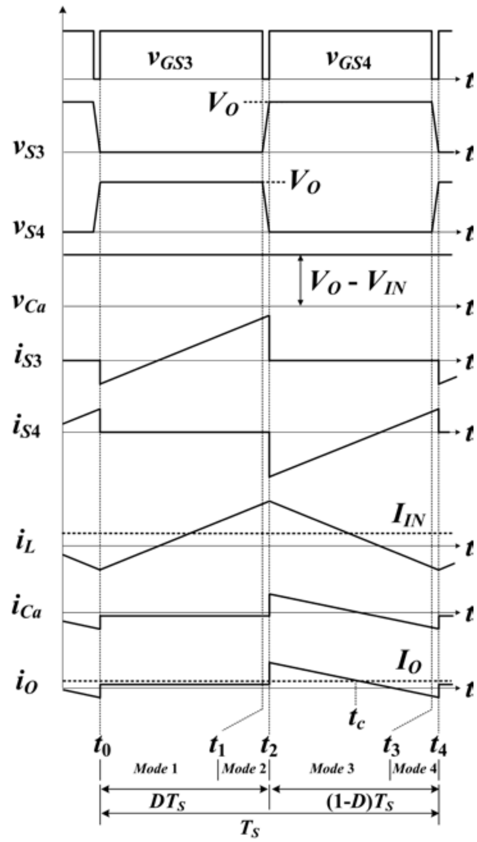

Fig. 8. Operational waveforms in the operation of boost.

waveforms are shown in Fig. 9 and Fig. 10, respectively.

Mode 1 (Fig. 9(a), $t_0 \le t \le t_1$) starts when S_2 and S_3 are turned on. At $t = t_0$, S_2 and S_3 achieve ZVS turn-on because D_{S2} and D_{S3} are turned on before $t = t_0$. Then, v_L becomes V_{IN}, and i_L is expressed as

$$i_L(t) = i_L(t_0) + \frac{V_{IN}}{L}(t - t_0). \quad (17)$$

Both i_{S2} and i_{S3} are same as i_L, so they are expressed as

$$i_{S2}(t) = i_{S3}(t) = i_L(t_0) + \frac{V_{IN}}{L}(t - t_0).$$

Because $i_O = -i_{Ca}$, $i_O = i_{Co} + I_O$, and $i_{Co} = i_{Ca} \cdot C_O/C_a$, i_{Ca} and i_O are expressed as

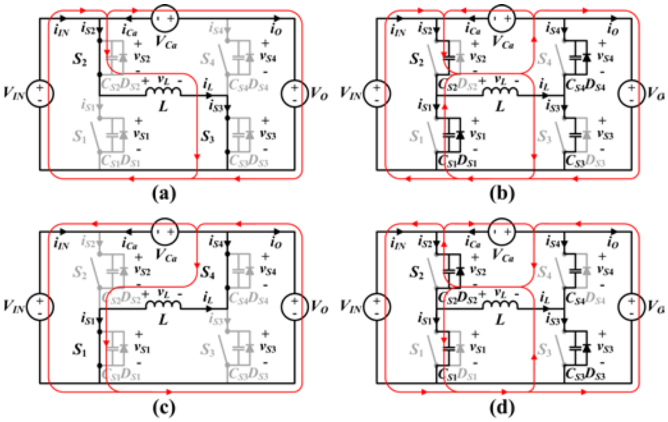

Fig. 9. Circuit diagrams for the operation of buck-boost; (a) *Mode* 1, (b) *Mode* 2, (c) *Mode* 3, and (d) *Mode* 4.

$$i_{Ca}(t) = -\frac{C_a}{C_a + C_O} I_O \tag{18}$$

$$i_O(t) = \frac{C_a}{C_a + C_O} I_O . \tag{19}$$

$v_{Ca}(t)$ is obtained using the equation (18) as

$$v_{Ca}(t) = v_{Ca}(t_0) + \frac{1}{C_a}\int_{t_0}^{t} i_{Ca}(t)dt \approx v_{Ca} + \frac{1}{C_a}\left[\frac{-C_a I_O}{C_a + C_O}(t - t_0)\right]$$

$$= V_O - V_{IN} - \frac{I_O}{C_a + C_O}(t - t_0).$$

Mode 2 (Fig. 9(b), $t_1 \le t \le t_2$) starts when S_2 and S_3 are turned off and S_1 and S_4 remain in the off state. In this mode, C_{S2} and C_{S3} charge from 0 to V_{IN} and from 0 to V_O, respectively. C_{S1} and C_{S4} discharge from V_{IN} to 0 and from V_O to 0, respectively. Shortly after the charging and discharging processes are finished, the D_{S1} and D_{S4} are turned on.

Mode 3 (Fig. 9(c), $t_2 \le t \le t_3$) starts with the ZVS turn-on of S_1 and S_4 because D_{S1} and D_{S4} are turned on before $t = t_2$. Then, v_L becomes $-V_O$, and i_L is expressed as

$$i_L(t) = i_L(t_2) - \frac{V_O}{L}(t - t_2). \tag{20}$$

i_{S1} and i_{S4} are equal to $-i_L$, so they are obtained as

$$i_{S1}(t) = i_{S4}(t) = -i_L(t_2) + \frac{V_O}{L}(t - t_2).$$

Because $i_O = i_L - i_{Ca}$, $i_O = i_{Co} + I_O$, and $i_{Co} = i_{Ca} \cdot C_O / C_a$, i_{Ca} and i_O are expressed as

$$i_{Ca}(t) = \frac{C_a}{C_a + C_O}\left[i_L(t) - I_O\right] \tag{21}$$

$$i_O(t) = \frac{C_O}{C_a + C_O} i_L(t) + \frac{C_a}{C_a + C_O} I_O . \tag{22}$$

v_{Ca} is obtained using equations (20) and (21) as

$$v_{Ca}(t) = \frac{1}{C_a}\int_{t_2}^{t} i_{Ca}(t)dt + v_{Ca}(t_2)$$

$$= \frac{1}{C_a + C_O}\left[(i_L(t_2) - I_O)(t - t_2) - \frac{V_O}{2L}(t - t_2)^2\right] + v_{Ca}(t_2).$$

Mode 4 (Fig. 9(d), $t_3 \le t \le t_4$) starts when S_1 and S_4 are turned off and S_2 and S_3 remain in the off state. In this mode, C_{S2} and C_{S3} discharge from V_{IN} to 0 and from V_O to 0, respectively. C_{S1} and C_{S4} charge from 0 to V_{IN} and from 0 to V_O, respectively. Shortly after the discharging and charging processes are finished, D_{S2} and D_{S3} are turned on.

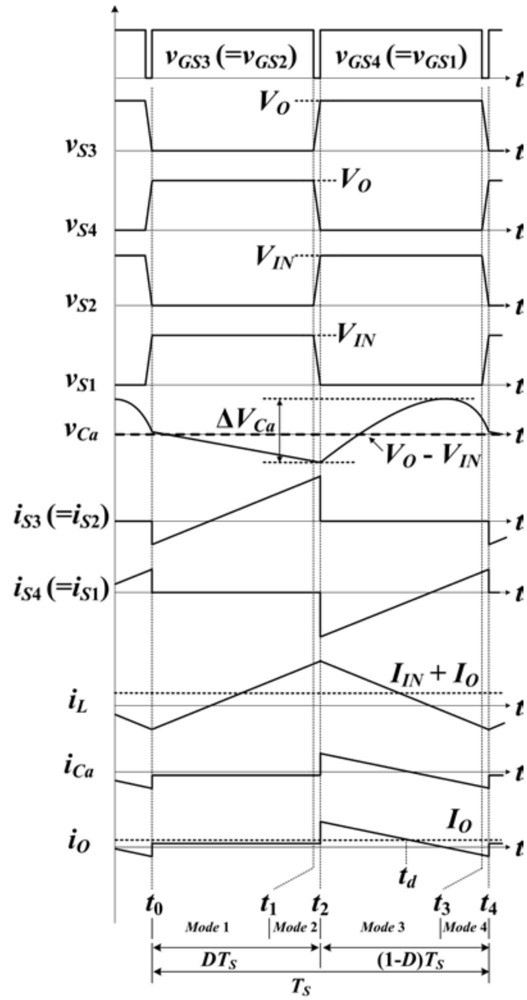

Fig. 10. Operational waveforms in the operation of buck-boost.

By inserting $t = t_2$ into (17), Δi_L is obtained for buck-boost operation as

$$\Delta i_L = i_L(t_2) - i_L(t_0) = \frac{V_{IN}}{L} DT_S , \tag{23}$$

where $DT_S = t_2 - t_0$. Because $\langle i_L \rangle = I_{IN} + I_O$ and $i_L(t_0) = \langle i_L \rangle - \Delta i_L/2$, $i_L(t_0)$ is expressed as

$$i_L(t_0) = I_{IN} + I_O - \frac{V_{IN}}{2L} DT_S , \tag{24}$$

and $i_L(t_2) = \langle i_L \rangle + \Delta i_L/2$ is expressed as

$$i_L(t_2) = I_{IN} + I_O + \frac{V_{IN}}{2L} DT_S . \tag{25}$$

C. Voltage Gain

When the proposed converter operates in buck mode, v_L becomes $V_{IN} - V_O$ for $t_0 \le t \le t_2$ and $-V_O$ for $t_2 \le t \le t_4$. Therefore, the volt-second balance law for L results in

$$\frac{V_O}{V_{IN}} = D , \tag{26}$$

where $DT_S = t_2 - t_0$ and $(1 - D)T_S = t_4 - t_2$.

In boost mode, v_L becomes V_{IN} for $t_0 \le t \le t_2$ and $V_{IN} - V_O$ for $t_2 \le t \le t_4$. Therefore, the volt-second balance law for L results in

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$$\frac{V_O}{V_{IN}} = \frac{1}{1-D}, \tag{27}$$

where $DT_S = t_2 - t_0$ and $(1 - D)T_S = t_4 - t_2$.

In buck-boost mode, v_L becomes V_{IN} for $t_0 \le t \le t_2$ and $-V_O$ for $t_2 \le t \le t_4$. Therefore, the volt-second balance law for L results in

$$\frac{V_O}{V_{IN}} = \frac{D}{1-D}, \tag{28}$$

where $DT_S = t_2 - t_0$ and $(1 - D)T_S = t_4 - t_2$.

D. Output Voltage Ripple

When the proposed converter operates in buck mode, the output voltage ripple Δv_o is expressed as

$$\Delta v_o = \frac{1}{C_O}\int_{t_a}^{t_b} i_{Co}(t)dt. \tag{29}$$

For $t_0 \le t \le t_2$, i_{Co} is obtained using (1), (2), $i_O = i_{Co} + I_O$, and (7) as

$$i_{Co}(t) = \frac{C_O(V_{IN} - V_O)}{L(C_a + C_O)}\left[(t - t_0) - \frac{DT_S}{2}\right]. \tag{30}$$

For $t_2 \le t < t_4$, the equations (3), (5), $i_O = i_{Co} + I_O$, and (8) result in

$$i_{Co}(t) = \frac{C_O}{C_a + C_O}\left[\frac{-V_O}{L}(t - t_2) + \frac{V_{IN} - V_O}{2L}DT_S\right]. \tag{31}$$

As shown in Fig. 6, $i_{Co}(t) = 0$ (or $i_O(t) = I_O$) occurs at $t = t_a$ and $t = t_b$. By inserting $t = t_a$ into (30), t_a is obtained as

$$t_a = t_0 + \frac{DT_S}{2}, \tag{32}$$

and t_b is obtained by inserting $t = t_b$ into (31) as follows

$$t_b = t_2 + \frac{V_{IN} - V_O}{2V_O}DT_S.$$

Using (26), this equation can be represented as

$$t_b = t_2 + \frac{(1-D)T_S}{2}. \tag{33}$$

Then, Δv_o is obtained using (26), (29), (31), (32), and (33) as

$$\Delta v_o = \frac{V_O(1-D)T_S^{\,2}}{8L(C_a + C_O)}. \tag{34}$$

When the proposed converter operates in boost mode, Δv_o is expressed as

$$\Delta v_o = \frac{1}{C_O}\int_{t_2}^{t_c} i_{Co}(t)dt. \tag{35}$$

For $t_2 \le t < t_4$, the equations (11), (13), $i_O = i_{Co} + I_O$, and (16) result in

$$i_{Co}(t) = \frac{C_O}{C_a + C_O}\left[I_{IN} + \frac{V_{IN} - V_O}{L}(t - t_2) + \frac{V_{IN}}{2L}DT_S - I_O\right]. \tag{36}$$

As shown in Fig. 8, $i_{Co}(t)$ becomes 0 at $t = t_2$ and $t = t_c$. By inserting $t = t_c$ into (36), t_c is obtained as

$$t_c = t_2 + \frac{(I_{IN} - I_O)L + V_{IN}DT_S/2}{V_O - V_{IN}}. \tag{37}$$

Then, Δv_o is obtained using (35), (36), and (37) as

$$\Delta v_o = \frac{[(I_{IN} - I_O)L + V_{IN}DT_S/2]^2}{2L(C_a + C_O)(V_O - V_{IN})}. \tag{38}$$

In buck-boost operation, Δv_o is expressed as

$$\Delta v_o = \frac{1}{C_O}\int_{t_2}^{t_d} i_{Co}(t)dt. \tag{39}$$

For $t_2 \le t < t_4$, equations (20), (22), $i_O = i_{Co} + I_O$, and (25) result in

$$i_{Co}(t) = \frac{C_O}{C_a + C_O}\left[I_{IN} - \frac{V_O}{L}(t - t_2) + \frac{V_{IN}}{2L}DT_S\right]. \tag{40}$$

As shown in Fig. 10, $i_{Co}(t)$ becomes 0 at $t = t_2$ and $t = t_d$. By inserting $t = t_d$ into (40), t_d is obtained as

$$t_d = t_2 + \frac{LI_{IN} + V_{IN}DT_S/2}{V_O}. \tag{41}$$

Then, Δv_o is obtained using (39), (40), and (41) as

$$\Delta v_o = \frac{(LI_{IN} + V_{IN}DT_S/2)^2}{2LV_O(C_a + C_O)}. \tag{42}$$

E. Loss Analysis

The five main causes of power dissipation in the proposed converter include the switching and conduction losses of switches, the winding and core losses of inductor L, and the equivalent series resistance (ESR) losses of the capacitors [31-33].

The Switching loss of a switch ($P_{SW,swit}$) usually includes turn-on loss, turn-off loss, reverse recovery loss of the body-diode, and output capacitance loss. However, the proposed converter has only the turn-off and output capacitance losses because it achieves ZVS turn-on for the switches. The turn-off loss of switch is expressed as

$$P_{SW,turn-off} = \frac{1}{2}V_{SW,turn-off}I_{SW,turn-off}(T_1 + T_2)f_S, \tag{43}$$

where $T_1 = (V_{SW,turn-off}C_{gd}R_g)/(V_t + I_{SW,turn-off}/g)$, $T_2 = R_gC_g\ln(I_{SW,turn-off}/(gV_t)+1)$, $V_{SW,turn-off}$ and $I_{SW,turn-off}$ are the switch voltage and current at the instance of turn-off transition, C_{gd} is the gate-drain capacitance, R_g is the gate resistance, C_g is the gate capacitance, g is the transconductance, and V_t is the threshold voltage of a switch. The output capacitance loss of a switch is expressed as

$$P_{Cds} = \frac{1}{2}C_{ds}V_{SW,turn-off}^{\;\;2}f_S, \tag{44}$$

where C_{ds} is the output capacitance of the switch. The switching loss of the switch is expressed as

$$P_{SW,swit} = P_{SW,turn-off} + P_{Cds}. \tag{45}$$

The Conduction loss of a switch ($P_{SW,cond}$) is expressed as

$$P_{SW,cond} = I_{SW,rms}^{\;\;2}R_{on}, \tag{46}$$

where $I_{SW,rms}$ is the RMS value of the switch current, and R_{on} is the on-resistance of the switch.

The Winding loss of inductor ($P_{L,wind}$) is expressed as

$$P_{L,wind} = I_{L,rms}^{\;\;2}R_L, \tag{47}$$

where R_L is the winding resistance of the inductor.

The Core loss of inductor ($P_{L,core}$) is expressed as

$$P_{L,core} = kf_S^{\,x}B_{\max}^{\;\;y}(l_eA_e), \tag{48}$$

where k, x, and y are the coefficient of core loss, maximum flux density B_{max} is $B_{\max} = L\Delta i_L/(NA_e)$, N is the number of turns, l_e is the effective magnetic path length of the core, A_e is the effective cross-sectional area of the core.

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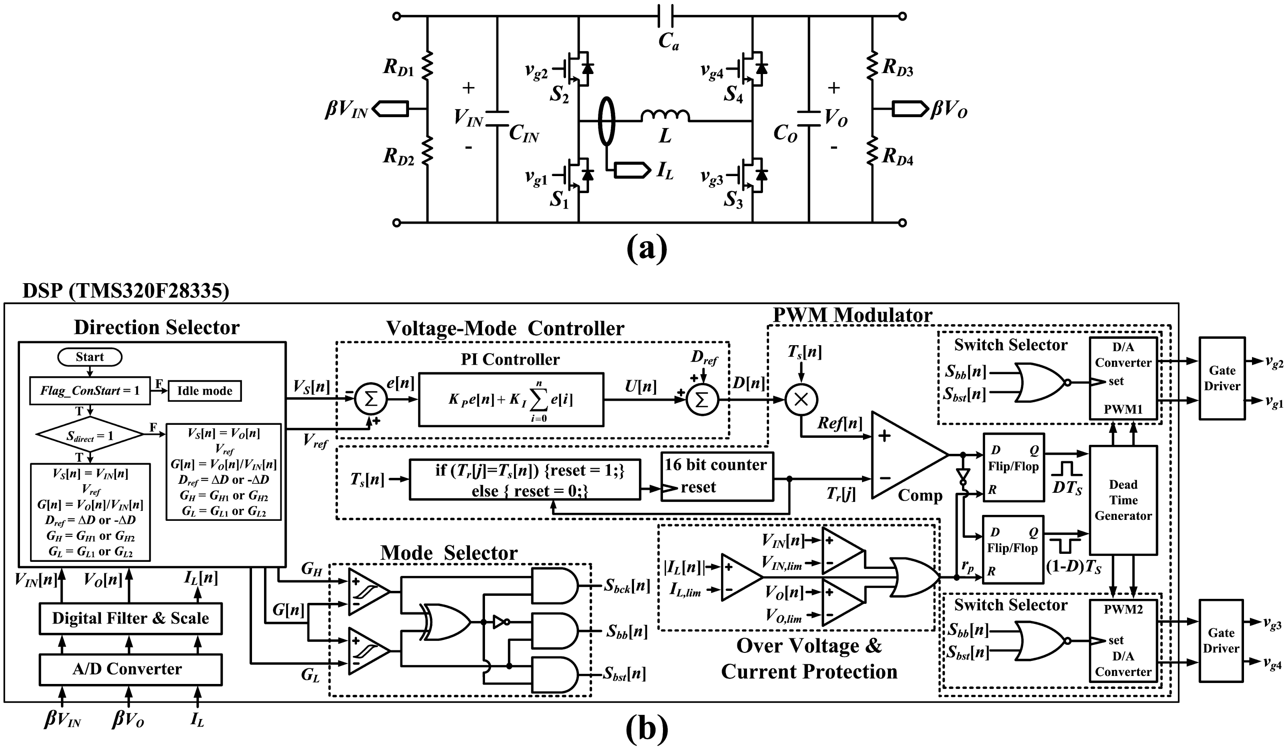

Fig. 11. (a) Circuit structure of the proposed converter with the voltage and current sensing (βV_{IN}, βV_O, and I_L), (b) Block diagram of the digital controller for the proposed converter.

The ESR loss of capacitor ($P_{C,ESR}$) is expressed as

$$P_{C,ESR} = I_{C,rms}{}^2 R_C\,, \tag{49}$$

where $I_{C,rms}$ is the RMS value of the capacitor current, and R_C is the ESR of the capacitor.

The voltages and currents of the key power components for calculating these power losses have different values for the different operating modes (Table II). The theoretical efficiency of the proposed converter can be calculated by inserting voltage and current values into the equations (43 ~ 49) related to the power loss calculations.

F. Operation of the Controller

The proposed converter is controlled by pulse width modulation (PWM) signals (v_{g1} ~ v_{g4}), which are generated by the voltage-mode control (Fig. 11(a)). Two voltages (V_{IN} and V_O) are sensed to implement the voltage-mode control and protect the over voltage. V_O is used as an output voltage for generating the PWM control signal of the main switch in the energy transfer direction from V_{IN} to V_O, and V_{IN} is used as an output voltage in the opposite direction. The current of inductor is sensed to protect against over current.

Fig. 11(b) represents a block diagram of the digital controller for the proposed converter. When the energy transfer direction is expressed by the demand of the system, the direction selector determines the sensing output voltage (V_{IN} or V_O) needed for the voltage mode control. The voltage-mode PI controller then generates the duty ratio D of the main switch by comparing the sensed voltage with the reference voltage. The mode selector informs the PWM modulator of the operating mode of the proposed converter determined by the sensed V_{IN} and V_O. Finally, using the information from the mode selector and voltage mode controller, the PWM modulator and the switch selector generates four gate signals (v_{g1} ~ v_{g4}), which control the proposed converter.

TABLE II
VOLTAGE AND CURRENT OF THE KEY POWER COMPONENTS FOR CALCULATING FIVE MAIN CAUSES OF POWER DISSIPATION

Five main causes of power dissipation	Operating modes		
	Buck mode	Boost mode	Buck-Boost mode
Switching loss of switch	$V_{S1,turn-off} = V_{S2,turn-off} = V_{IN}$ $I_{S1,turn-off} = -I_O + \frac{V_{IN}-V_O}{2L}DT_S$ $I_{S2,turn-off} = I_O + \frac{V_{IN}-V_O}{2L}DT_S$	$V_{S3,turn-off} = V_{S4,turn-off} = V_O$ $I_{S3,turn-off} = I_{IN} + \frac{V_{IN}}{2L}DT_S$ $I_{S4,turn-off} = -I_{IN} + \frac{V_{IN}}{2L}DT_S$	$V_{S1,turn-off} = V_{S2,turn-off} = V_{IN}$ $V_{S3,turn-off} = V_{S4,turn-off} = V_O$ $I_{S2,turn-off} = I_{S3,turn-off} = I_{IN} + I_O + \frac{V_{IN}}{2L}DT_S$ $I_{S1,turn-off} = I_{S4,turn-off} = -I_{IN} - I_O + \frac{V_{IN}}{2L}DT_S$
Conduction loss of switch	$I_{S1,rms} = \sqrt{1-D}I_{L,rms}$ $I_{S2,rms} = \sqrt{D}I_{L,rms}$ $I_{S4,rms} = I_{L,rms}$	$I_{S3,rms} = \sqrt{D}I_{L,rms}$ $I_{S4,rms} = \sqrt{1-D}I_{L,rms}$ $I_{S1,rms} = I_{L,rms}$	$I_{S1,rms} = \sqrt{1-D}I_{L,rms}$ $I_{S2,rms} = \sqrt{D}I_{L,rms}$ $I_{S3,rms} = \sqrt{D}I_{L,rms}$ $I_{S4,rms} = \sqrt{1-D}I_{L,rms}$
Winding loss of inductor	$I_{L,rms} = \sqrt{I_O{}^2 + \frac{V_{IN}-V_O}{12L}DT_S}$	$I_{L,rms} = \sqrt{I_{IN}{}^2 + \frac{V_{IN}}{12L}DT_S}$	$I_{L,rms} = \sqrt{(I_{IN}+I_O)^2 + \frac{V_{IN}}{12L}DT_S}$
Core loss of inductor	$\Delta i_L = \frac{V_{IN}-V_O}{L}DT_S$	$\Delta i_L = \frac{V_{IN}}{L}DT_S$	$\Delta i_L = \frac{V_{IN}}{L}DT_S$
ESR loss of capacitor	$I_{Ca,rms} = I_{Co,rms} = \frac{V_{IN}-V_O}{4\sqrt{3}L}DT_S$	$I_{Ca,rms} = I_{Co,rms} \approx \frac{1}{2}\sqrt{1-D}I_{L,rms}$	$I_{Ca,rms} = I_{Co,rms} \approx \frac{1}{2}\sqrt{1-D}I_{L,rms}$

The proposed converter has six operating conditions that depend on the energy transfer direction and operating modes (Table I). In each energy transfer direction, one of three operating modes is used (buck, boost, or buck-boost), which depends on the relationship between V_{IN} and V_O. However, the operation of the converter can be unstable because abrupt transitions occur between the modes (buck ↔ buck-boost or

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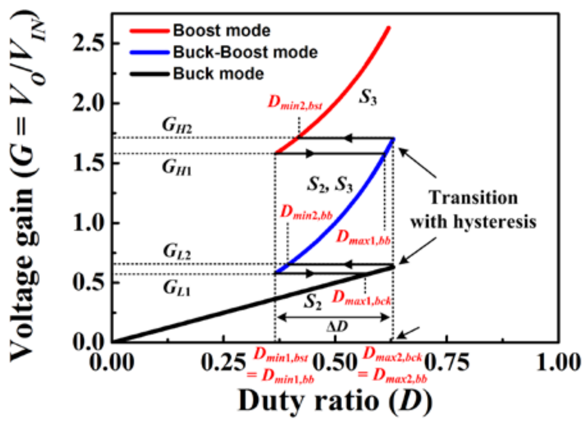

Fig. 12. Voltage gain versus duty ratio of the proposed converter.

buck-boost ↔ boost). Hysteresis control and the switch selector are used to solve this problem. The hysteresis control uses different gains (G_{L1}, G_{L2}, G_{H1}, G_{H2}) for smooth transition between modes, and the switch selector determines the main switch that controls the operation and voltage gain G (= V_O / V_{IN}) of the converter in each mode (Fig. 12).

The hysteresis control is explained in the following for operating mode transitions.

1) *Transition from buck mode to buck-boost mode*

The transition from buck mode to buck-boost mode occurs at $G = G_{L2}$ (@ $D = D_{max2,bck}$). For buck-boost mode, S_1, S_2, S_3, and S_4 have duty ratios of 1-D, D, D, and 1-D, respectively, and S_2 becomes the main switch. The duty ratio D of S_2 is decreased from $D_{max2,bck}$ to $D_{min2,bb}$ so that the proposed converter has a voltage gain G of G_{L2} in buck-boost mode.

2) *Transition from buck-boost mode to boost mode*

The transition from buck-boost mode to boost mode occurs at $G = G_{H2}$ (@ $D = D_{max2,bb}$). For boost mode, S_1, S_2, S_3, and S_4 have duty ratios of 0, 1, D, and 1-D, respectively, and S_3 becomes the main switch. The duty ratio D of S_3 is decreased from $D_{max2,bb}$ to $D_{min2,bst}$ so that the proposed converter has a voltage gain G of G_{H2} in the boost mode.

3) *Transition from boost mode to buck-boost mode*

The transition from the boost mode to the buck-boost mode occurs at $G = G_{H1}$ (@ $D = D_{min1,bst}$). For buck-boost mode, S_1, S_2, S_3, and S_4 have duty ratios of 1-D, D, D, and 1-D, respectively, and S_3 becomes the main switch. The duty ratio D of S_3 is increased from $D_{min1,bst}$ to $D_{max1,bb}$ so that the proposed converter has a voltage gain G of G_{H1} in the buck-boost mode.

4) *Transition from buck-boost mode to buck mode*

The transition from the buck-boost mode to the buck mode occurs at $G = G_{L1}$ (@$D = D_{min1,bb}$). For buck mode, S_1, S_2, S_3, and S_4 have duty ratios of 1-D, D, 0, and 1, respectively, and S_2 becomes the main switch. The duty ratio D of S_2 is increased from $D_{min1,bb}$ to $D_{max1,bck}$ so that the proposed converter has a voltage gain G of G_{L1} in the buck mode.

In the opposite energy transfer direction ($V_O \rightarrow V_{IN}$), the transitions between different operating modes are controlled by the same method.

III. Design Considerations

A. Switches S_1, S_2, S_3, and S_4

The voltage stress for each switch is V_O or V_{IN}, depending on the position of the switch and operating modes. The proposed converter uses four identical power semiconductors as switches. Therefore, the voltage stress $v_{S,\max}$ for a switch is determined as a large value of V_{IN} and V_O.

The current stresses for the switches change according to the energy transfer directions and operating modes. The maximum current $i_{S,\max}$ of a switch is equal to $i_L(t_2)$, and is expressed in (8), (16), and (25) for buck, boost, and buck-boost operations.

The switch component should be chosen to satisfy $v_{S,\max} < V_{Switch}$ and $i_{S,\max} < I_{Switch}$, where V_{Switch} and I_{Switch} are the maximum voltage and current ratings of the switch component.

B. Inductor L

The proposed converter operates in DCM to achieve ZVS turn-on of the switches. To operate in DCM, the minimum value $i_L(t_0)$ of i_L should be smaller than 0. For buck operation, the condition $i_L(t_0) < 0$ and equation (7) result in

$$L < \frac{(V_{IN} - V_O)DT_S}{2I_{O,\max}}. \tag{50}$$

For boost operation, the condition for L is derived by inserting the condition $i_L(t_0) < 0$ into (15) as

$$L < \frac{V_{IN} DT_S}{2I_{IN,\max}}. \tag{51}$$

In buck-boost operation, the condition for L is derived by inserting the condition $i_L(t_0) < 0$ into (24) as

$$L < \frac{V_{IN} DT_S}{2(I_{IN,\max} + I_{O,\max})}. \tag{52}$$

L should be chosen to satisfy conditions (50) ~ (52).

C. Auxiliary Capacitor C_a

For a given allowed voltage ripple $\Delta v_{o,allow}$, the condition $\Delta v_{o,allow} > \Delta v_o$ and equation (34) result in the following condition in buck operation:

$$C_a > \frac{V_O(1-D)T_S^{\,2}}{8L\Delta v_{o,allow}} - C_O. \tag{53}$$

For boost operation, the condition for C_a is obtained using equation (38) under the condition $\Delta v_{o,allow} > \Delta v_o$:

$$C_a > \frac{\left(I_{IN} - I_O + \frac{V_{IN} DT_S}{2L}\right)\left[(I_{IN} - I_O)L + \frac{V_{IN} DT_S}{2}\right]}{2\Delta v_{o,allow}(V_O - V_{IN})} - C_O. \tag{54}$$

In buck-boost operation, the condition for C_a is obtained using the equation (42) under the condition $\Delta v_{o,allow} > \Delta v_o$:

$$C_a > \frac{(LI_{IN} + V_{IN} DT_S/2)^2}{2L\Delta v_{o,allow} V_O} - C_O. \tag{55}$$

C_a should satisfy conditions (53) ~ (55) to obtain low Δv_o for all operating ranges.

C_a has different current stresses in different operating modes. The current stresses for C_a in buck, boost, and buck-boost modes are obtained by inserting $t = t_2$ into equations (4), (12), and (21), respectively. The voltage stress $v_{Ca,\max}$ is $|V_O - V_{IN}|$.

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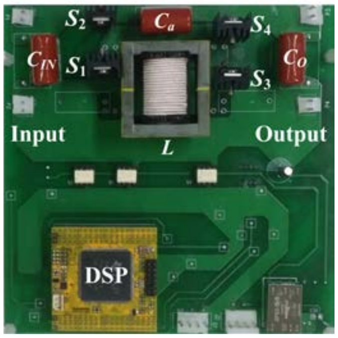

Fig. 13. Photograph of the proposed converter.

TABLE III
VALUES OF COMPONENTS FOR THE EXPERIMENTAL CONVERTERS

Components		Proposed converter	Coventional CBB converter
Core of inductor		EER 4042	EER 4042
Inductor (L)		184 μH	184 μH
Input capacitor (C_{IN})		3.3 μF	3.3 μF
Output capacitor (C_O)		3.3 μF	3.3 μF
Auxiliary capacitor (C_a)		3.3 μF	
Switches	(S_1)	STP28NM60	STP28NM60
	(S_2)	STP28NM60	STP28NM60
	(S_3)	STP28NM60	STP28NM60
	(S_4)	STP28NM60	STP28NM60

IV. EXPERIMENTAL RESULTS

The proposed converter (Fig. 13) with the digital controller in the digital signal processor (DSP) was designed to operate at V_{IN} = 160 V, V_O = 80 ~ 320 V, P_O = 16 ~ 160 W, and f_S = 45 kHz. From conditions (50), (51), and (52), L = 184 μH was determined to operate in DCM. C_a = 3.3 μF was determined by inserting $\Delta v_{o,allow} = 0.04V_{O,min}$ = 3.2 V and C_O = 3.3 μF into conditions (53) ~ (55). The proposed converter was built using the components and circuit parameters in Table III. In addition, a conventional CBB converter of [28] was built with the same specifications for comparison.

The waveforms of i_L, V_{Ca}, V_{IN}, and V_O in two energy transfer directions ($V_{IN} \rightarrow V_O$ and $V_O \rightarrow V_{IN}$) were measured at V_{IN} = 160 V, V_O = 80 V ~ 320 V, and P_O = 160 W (Fig. 14). Regardless of the energy transfer directions, the value of V_{Ca} was measured as $V_O - V_{IN}$ in buck and boost modes and was measured as the ripple voltage of C_a in buck-boost mode.

The voltage and current waveforms of the switches for the proposed converter were measured at V_{IN} = 160 V, V_O = 80 ~ 320 V, and P_O = 16 W (Fig. 15). Fig. 15(a), (c), and (e) present the switch waveforms in the energy transfer direction from V_{IN} to V_O. Fig. 15(b), (d), and (f) present the switch waveforms in the energy transfer direction from V_O to V_{IN}. At V_O = 80 V, the proposed converter operated in buck mode, and the voltage stresses of the switches were 160 V (Fig. 15(a)). At V_O = 160 V, the voltage stresses of the switches were 160 V because the proposed converter operated in buck-boost mode (Fig. 15(e)). At V_O = 320 V, the voltage stresses of the switches were 320 V because the proposed converter operated in boost mode (Fig. 15(c)). In all operating modes, ZVS turn-on of the switches was achieved because the proposed converter is operated in DCM.

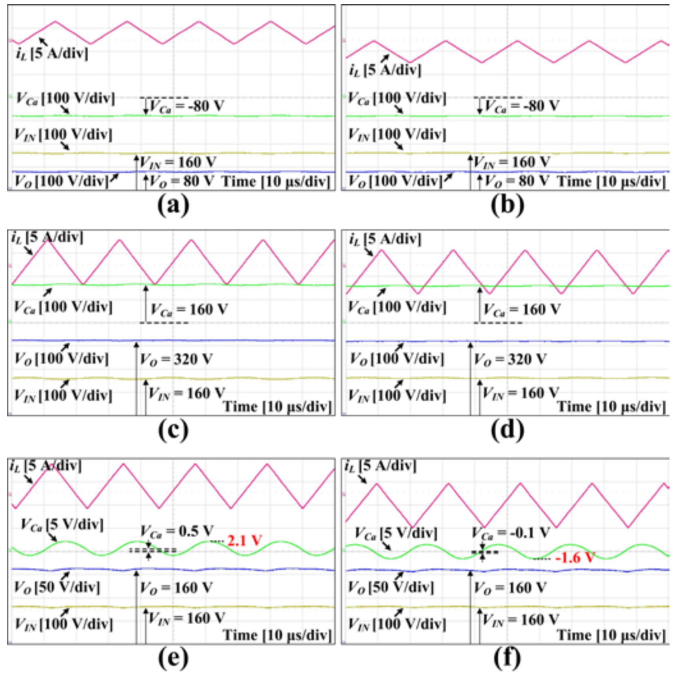

Fig. 14. The waveforms for i_L, V_{IN}, V_O, and V_{Ca} for the proposed converter measured at P_O = 160 W and the energy transfer directions from (a) V_{IN} = 160 V to V_O = 80 V, from (b) V_O = 80 V to V_{IN} = 160 V, from (c) V_{IN} = 160 V to V_O = 320 V, from (d) V_O = 320 V to V_{IN} = 160 V, from (e) V_{IN} = 160 V to V_O = 160 V, and from (f) V_O = 160 V to V_{IN} = 160 V.

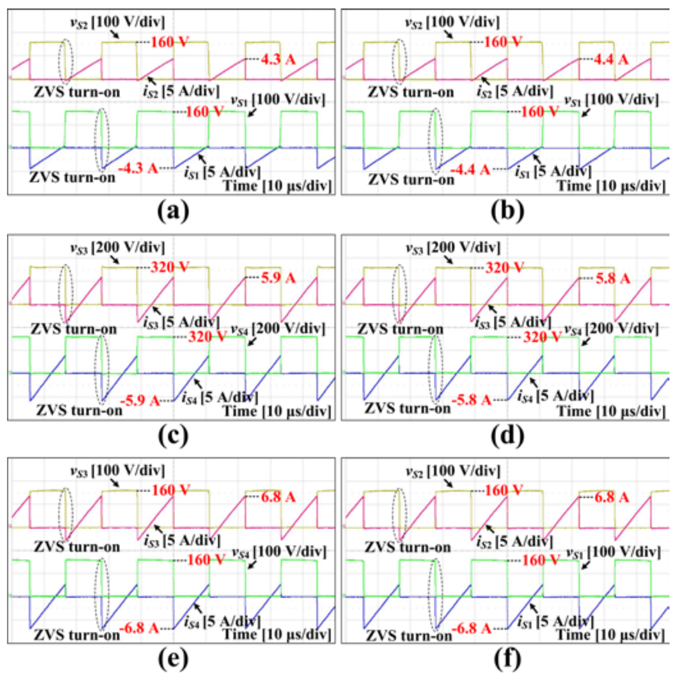

Fig. 15. The voltage and current waveforms for switches of the proposed converter measured at P_O = 160 W and the energy transfer directions from (a) V_{IN} = 160 V to V_O = 80 V, from (b) V_O = 80 V to V_{IN} = 160 V, from (c) V_{IN} = 160 V to V_O = 320 V, from (d) V_O = 320 V to V_{IN} = 160 V, from (e) V_{IN} = 160 V to V_O = 160 V, and (f) V_O = 160 V to V_{IN} = 160 V.

In the opposite direction, the switches were also operated with ZVS turn-on, and the voltage stresses of the switches became V_O or V_{IN} depending on the operating mode (Fig. 15(b), (d), and (f)).

The current i_L of L, the output voltage ripple Δv_o, and the output current ripple Δi_o of the proposed and conventional

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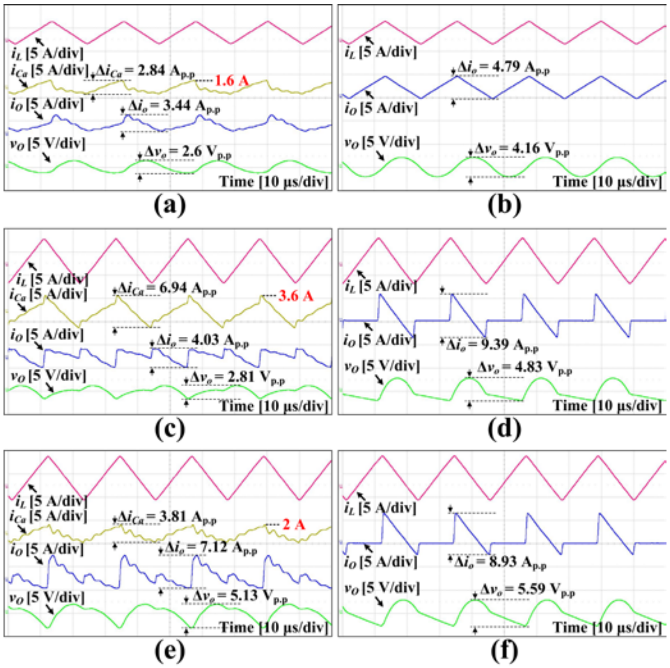

Fig. 16. The waveforms for i_L, Δv_o, and Δi_o for the proposed converter measured at P_O = 160 W and the energy transfer directions from (a) V_{IN} = 160 V to V_O = 80 V, from (c) V_{IN} = 160 V to V_O = 320 V, and from (e) V_{IN} = 160 V to V_O = 160 V; for the conventional converter measured at P_O = 160 W and the energy transfer directions from (b) V_{IN} = 160 V to V_O = 80 V, from (d) V_{IN} = 160 V to V_O = 320 V, and from (f) V_{IN} = 160 V to V_O = 160 V.

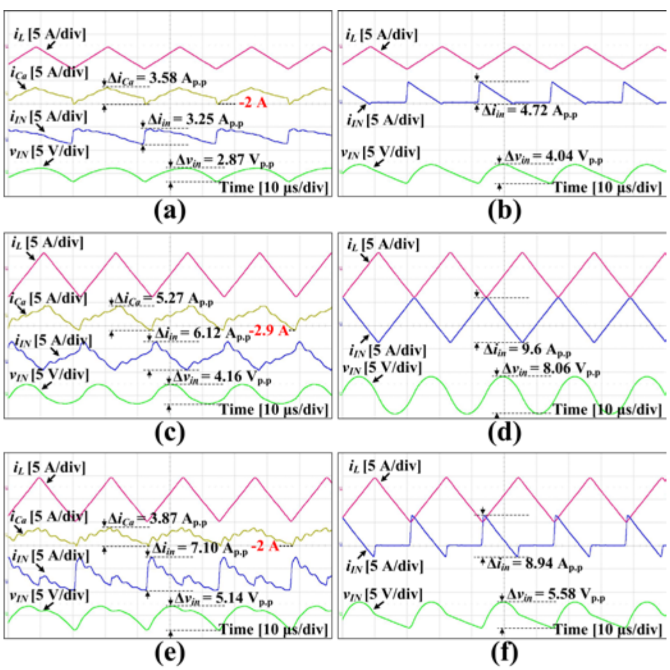

Fig. 17. The waveforms for i_L, Δv_{in}, and Δi_{in} for the proposed converter measured at P_O = 160 W and the energy transfer directions from (a) V_O = 80 V to V_{IN} = 160 V, from (c) V_O = 320 V to V_{IN} = 160 V, and from (e) V_O = 160 V to V_{IN} = 160 V; for the conventional converter measured at P_O = 160 W and the energy transfer directions from (b) V_O = 80 V to V_{IN} = 160 V, from (d) V_O = 320 V to V_{IN} = 160 V, and from (f) V_O = 160 V to V_{IN} = 160 V.

converters were measured at V_{IN} = 160 V, V_O = 80 V and 320 V, P_O = 160 W. The energy transfer direction was from V_{IN} to V_O (Fig. 16). Both the proposed and conventional converters had the same i_L because they used the same L. However, the proposed converter had lower Δv_o and Δi_o because it distributes

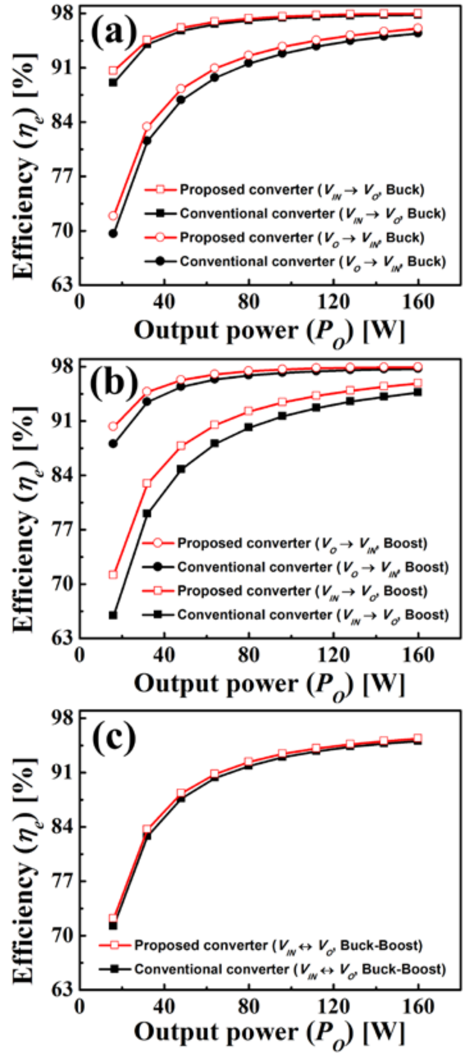

Fig. 18. Power-conversion efficiency versus output power for the proposed and conventional converters when operating in (a) buck mode, in (b) boost mode, and in (c) buck-boost mode.

i_L to C_a and C_O. When the energy transfer direction was from V_O to V_{IN} (Fig. 17), the proposed converter also had lower Δv_{in} and Δi_{in} than those of the conventional converter.

The power-conversion efficiency η_e of the proposed and conventional converters was measured at V_{IN} = 160 V, V_O = 80 ~ 320 V, and P_O = 16 ~ 160 W (Fig. 18). When operating in buck and boost mode (Fig. 18(a) and 18(b)), η_e of the proposed converter was higher than that of the conventional converter because the proposed converter had lower Δi_o than the conventional converter as a result of using C_a. However, when operating in buck-boost mode (Fig. 18(c)), η_e of the proposed converter was almost equal to that of the conventional converter because the proposed converter has similar Δi_o to that of the conventional converter in this mode.

η_e of the proposed converter was measured at V_{IN} = 160 V, V_O = 80 ~ 320 V, P_O = 16 and 160 W, and f_S = 45 ~ 135 kHz (Fig. 19). η_e decreases as f_S increases, and the maximum difference between the efficiencies measured at the operating frequencies of 45 kHz and 135 kHz is about 5% at P_O = 16 W. These results show that the proposed converter can achieve high η_e by

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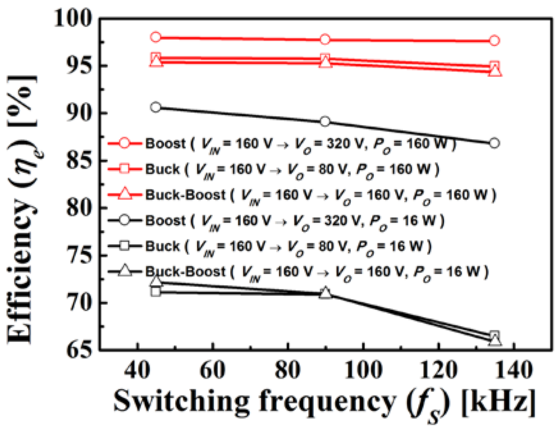

Fig. 19. Power-conversion efficiency versus switching frequency in the proposed converter.

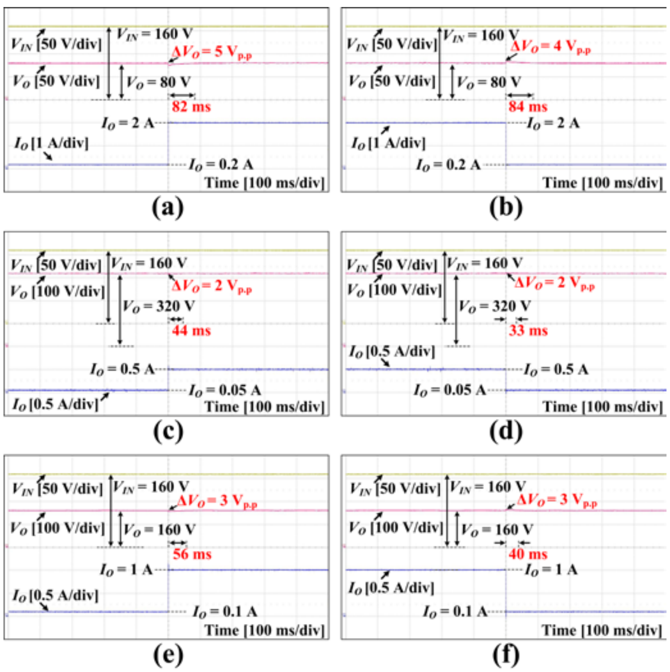

Fig. 20. Transient responses for the proposed converter while changing I_O (a) from 0.2 A to 2 A and (b) from 2 A to 0.2 A at the energy transfer direction from V_{IN} = 160 V to V_O = 80 V; (c) from 0.05 A to 0.5 A and (d) from 0.5 A to 0.05 A at the energy transfer direction from V_{IN} = 160 V to V_O = 320 V; (e) from 0.1 A to 1 A and (f) from 1 A to 0.1 A at the energy transfer direction from V_{IN} = 160 V to V_O = 160 V.

operating with low f_S.

The experimental transient responses (Fig. 20 and 21) to load changes of 10 ~ 100% for the proposed converter were measured depending with different energy transfer directions ($V_{IN} \rightarrow V_O$ or $V_O \rightarrow V_{IN}$) and three operating modes (buck, boost, and buck-boost modes). At the load transition, the maximum measured voltage spike was 9 $V_{p.p}$, and V_O returned to steady state within 17 ~ 128 ms after the load change. These results show that the proposed converter operated well for a sudden change in load conditions.

V. Conclusion

A new bidirectional buck-boost converter was proposed in this paper. The proposed converter effectively had lower output

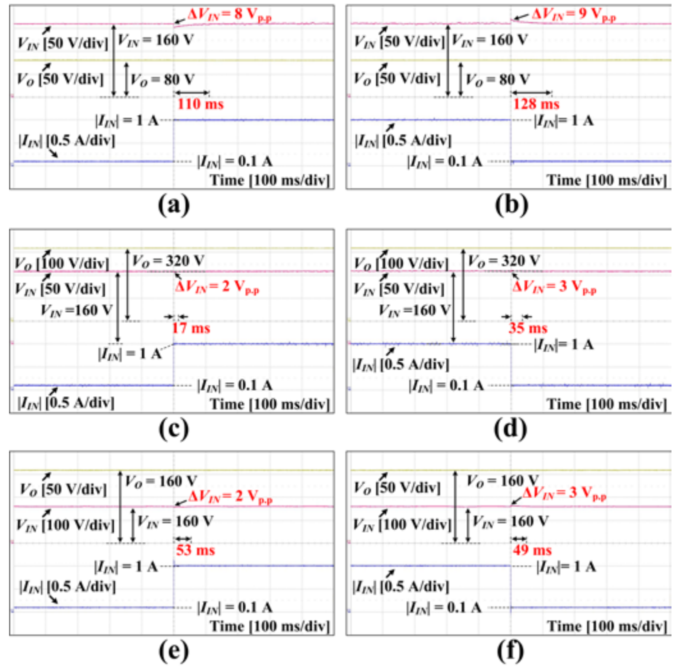

Fig. 21. Transient responses for the proposed converter while changing $|I_{IN}|$ (a) from 0.1 A to 1 A and (b) from 1 A to 0.1 A at the energy transfer direction from V_O = 80 V to V_{IN} = 160 V; (c) from 0.1 A to 1 A and (d) from 1 A to 0.1 A at the energy transfer direction from V_O = 320 V to V_{IN} = 160 V; (e) from 0.1 A to 1 A and (f) from 1 A to 0.1 A at the energy transfer direction from V_O = 160 V to V_{IN} = 160 V.

current ripple than the conventional CBB converter, which was achieved by providing a bypass path for the output current. The reduced output current ripple enabled lower output voltage ripple and higher power-conversion efficiency compared to the conventional converter. The proposed converter had a maximum efficiency of 98% at V_{IN} = 160 V, V_O = 80 ~ 320 V, P_O = 16 ~ 160 W, and f_S = 45 kHz, and the output voltage ripple was less than 5.14 $V_{p.p}$. These results show that the proposed converter is suitable for PV-ESS in a smart grid, which requires a bidirectional buck-boost converter with high efficiency and low ripples in the output voltage and current.

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